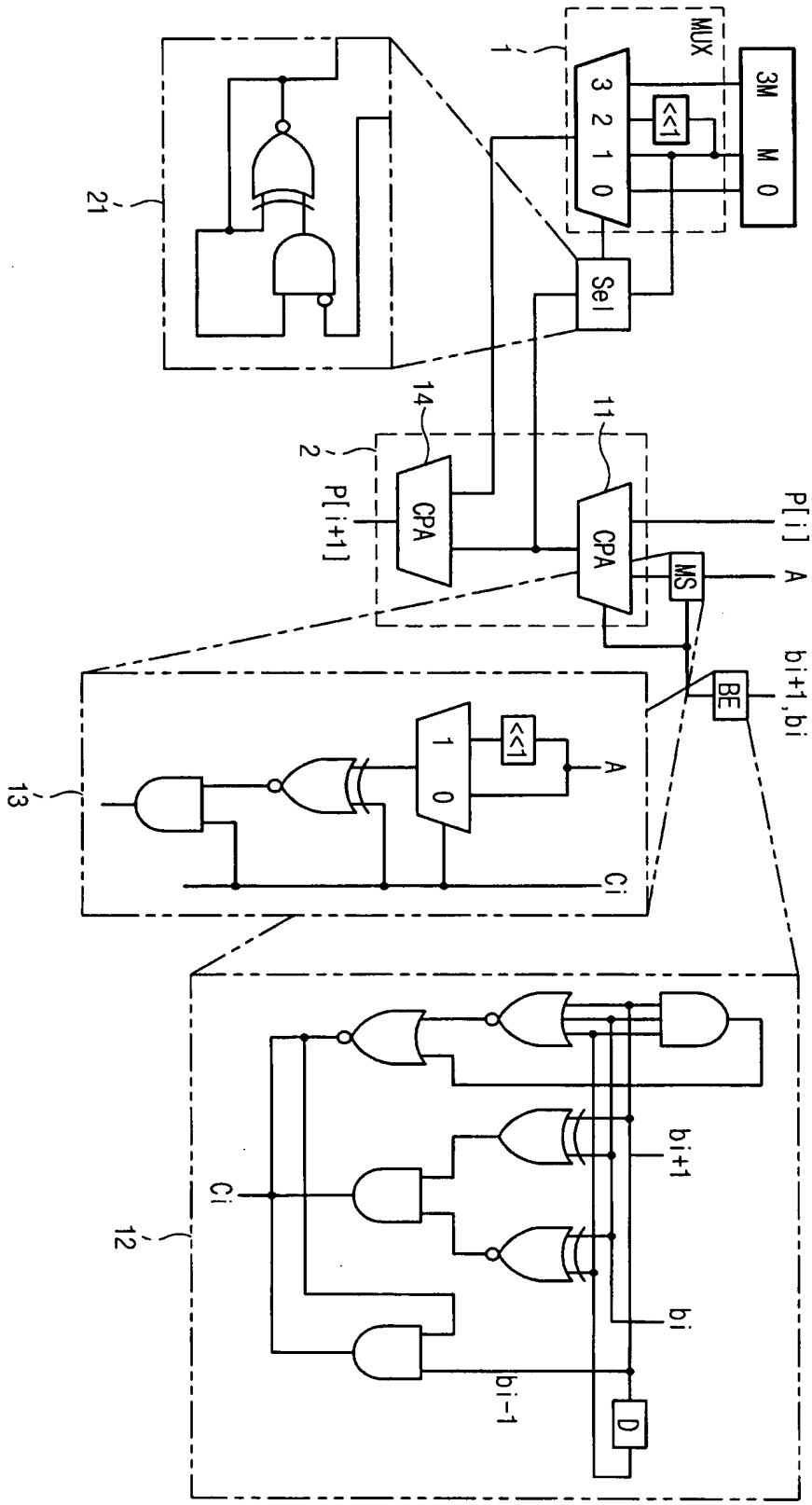

MUX
1
3M M 0
3 2 1 0
<<1
Sel
21
14
11
2
P[i+1]
CPA
CPA
P[i] A
MS
BE
bi+1,bi
13
1 0
<<1
A
Ci
12
Ci
bi+1
bi
bi-1
D

Fig. 1

Fig. 2

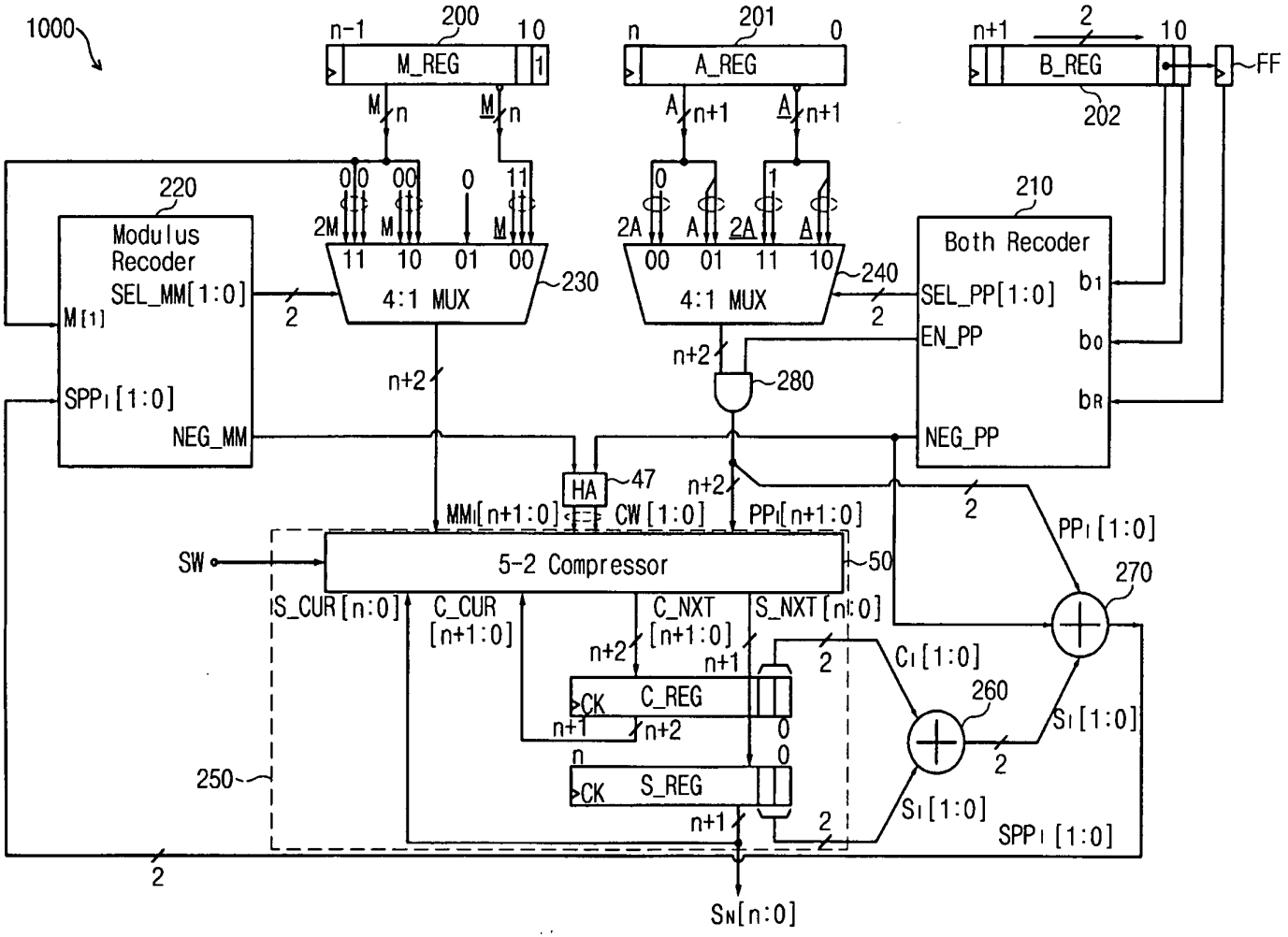

1000
M_REG
A_REG
B_REG
FF
202
Modulus Recoder
SEL_MM[1:0]
SPPI[1:0]
NEG_MM
4:1 MUX
4:1 MUX
Both Recoder
SEL_PP[1:0]
EN_PP
NEG_PP
HA
MMI[n+1:0]
CW[1:0]
PPI[n+1:0]
5-2 Compressor
SW
S_CUR[n:0]
C_CUR [n+1:0]
C_NXT [n+1:0]
S_NXT[n:0]
C_REG
S_REG
CI[1:0]
SI[1:0]
SPPI[1:0]
SN[n:0]

Fig. 3

Inputs of MR(220)			Outputs of MR(220)		Selected $MM_I[n+1:0]$
$SPP_I[1]$	$SPP_I[0]$	M[1]	SEL_MM[1:0]	NEG_MM	
0	0	0	11	0	0
0	0	1	11	0	0
0	1	0	01	1	M
0	1	1	00	0	M
1	0	0	10	0	2M
1	0	1	10	0	2M
1	1	0	00	0	M
1	1	1	01	1	M

Fig. 4

Inputs of BR(210)			Outputs of BR(210)			Selected $PP_I[n+1:0]$
b_I	b_0	b_R	SEL_PP[1:0]	EN_PP	NEG_PP	
0	0	0	Don't care	0	0	0
0	0	1	00	1	0	A
0	1	0	00	1	0	A
0	1	1	10	1	0	2A
1	0	0	11	1	1	$\underline{2A}$
1	0	1	01	1	1	$\underline{A}$
1	1	0	01	1	1	$\underline{A}$
1	1	1	Don't care	0	0	0

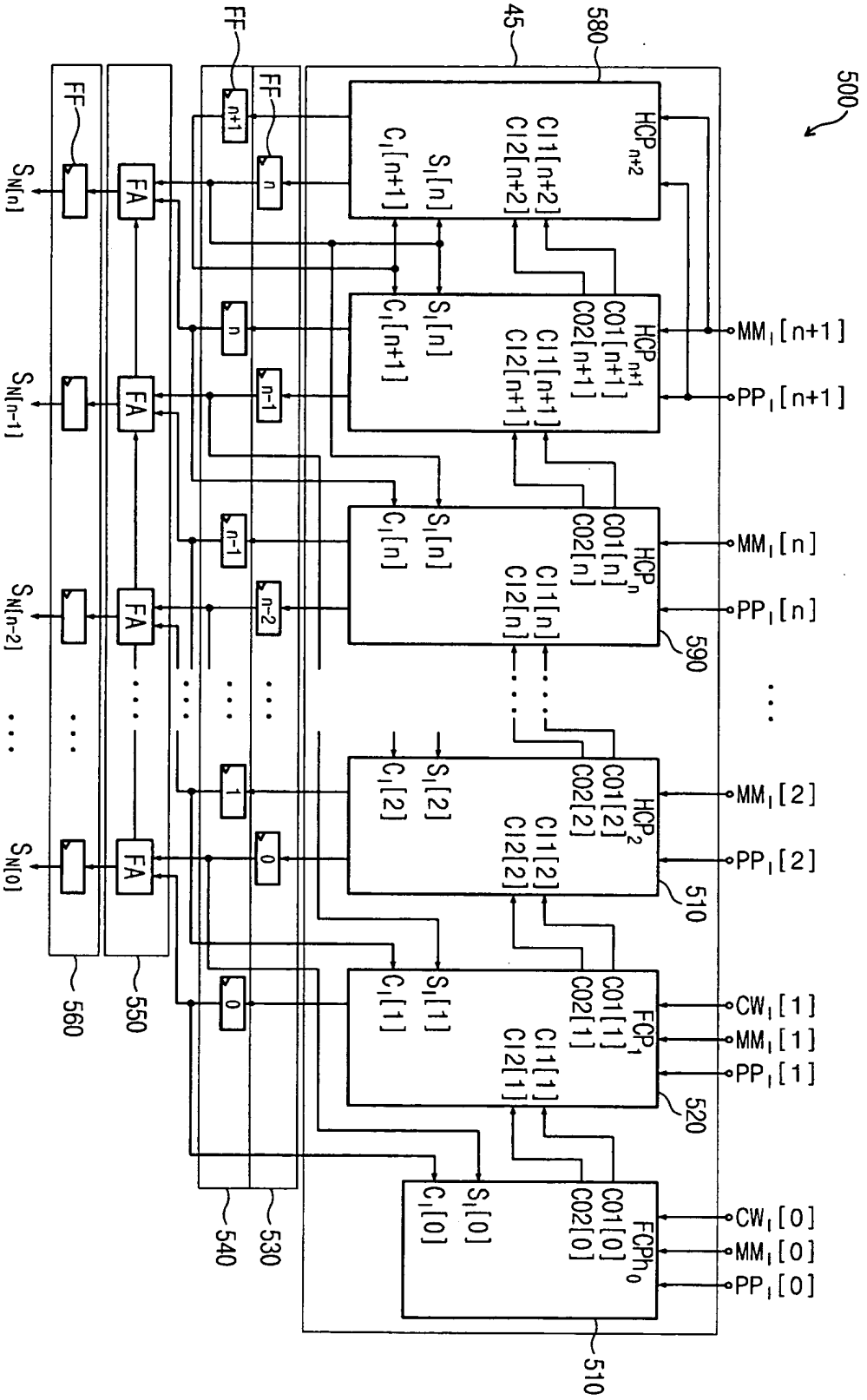

500
45
580
590
510
520
530
540
550
560
FF
FA
HCP n+2
HCP n+1
HCP n
HCP 2
FCP 1
FCPh 0
CI1[n+2]
CI2[n+2]
Si[n]
Ci[n+1]
CO1[n+1]
CO2[n+1]
CO1[n]
CO2[n]
CO1[2]
CO2[2]
Si[2]
Ci[2]
Si[1]
Ci[1]
CO1[1]
CO2[1]
Si[0]
Ci[0]
CO1[0]
CO2[0]
MMi[n+1]
PPi[n+1]
MMi[n]
PPi[n]
MMi[2]
PPi[2]
CWi[1]
MMi[1]
PPi[1]
CWi[0]
MMi[0]
PPi[0]
SN[n]
SN[n-1]
SN[n-2]
SN[0]

Fig. 5

Fig. 6

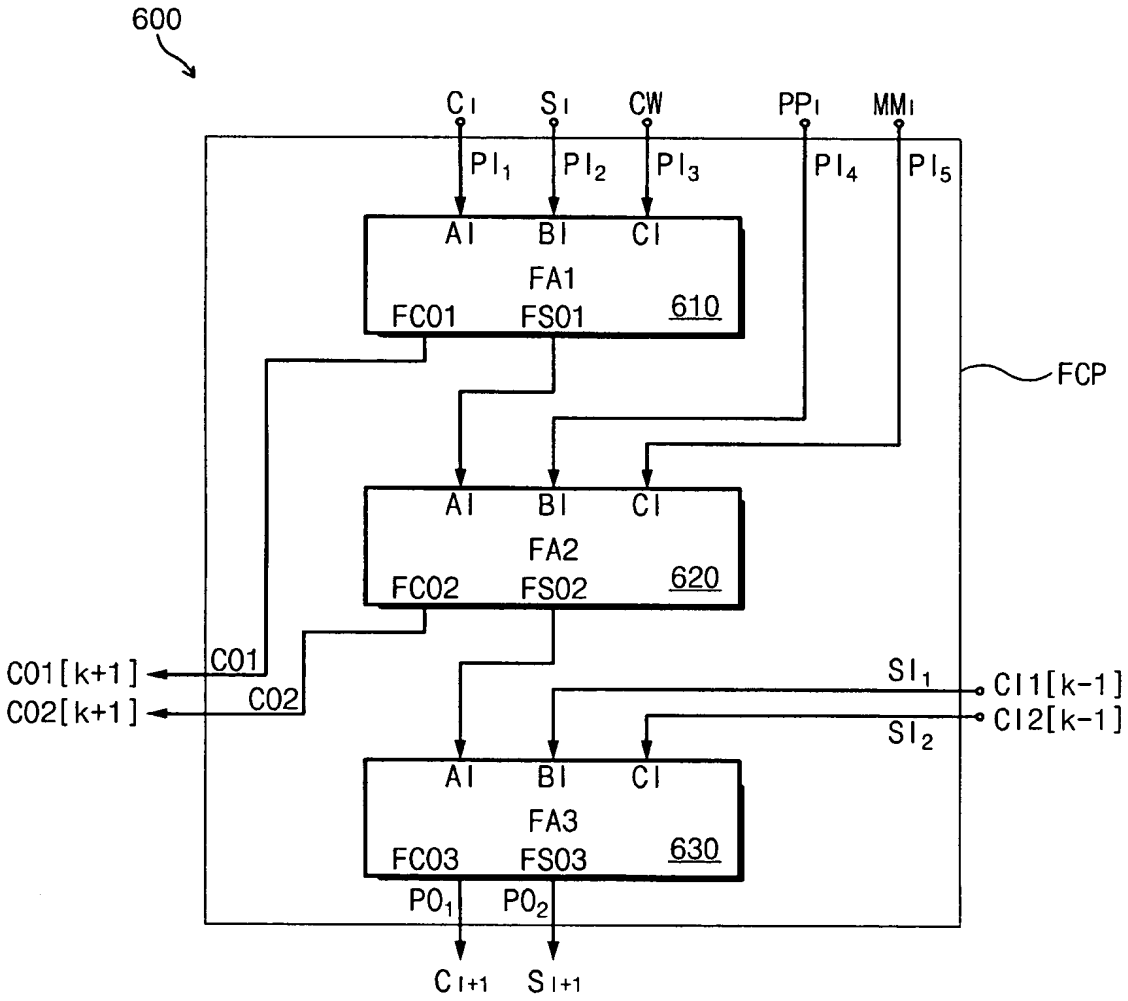
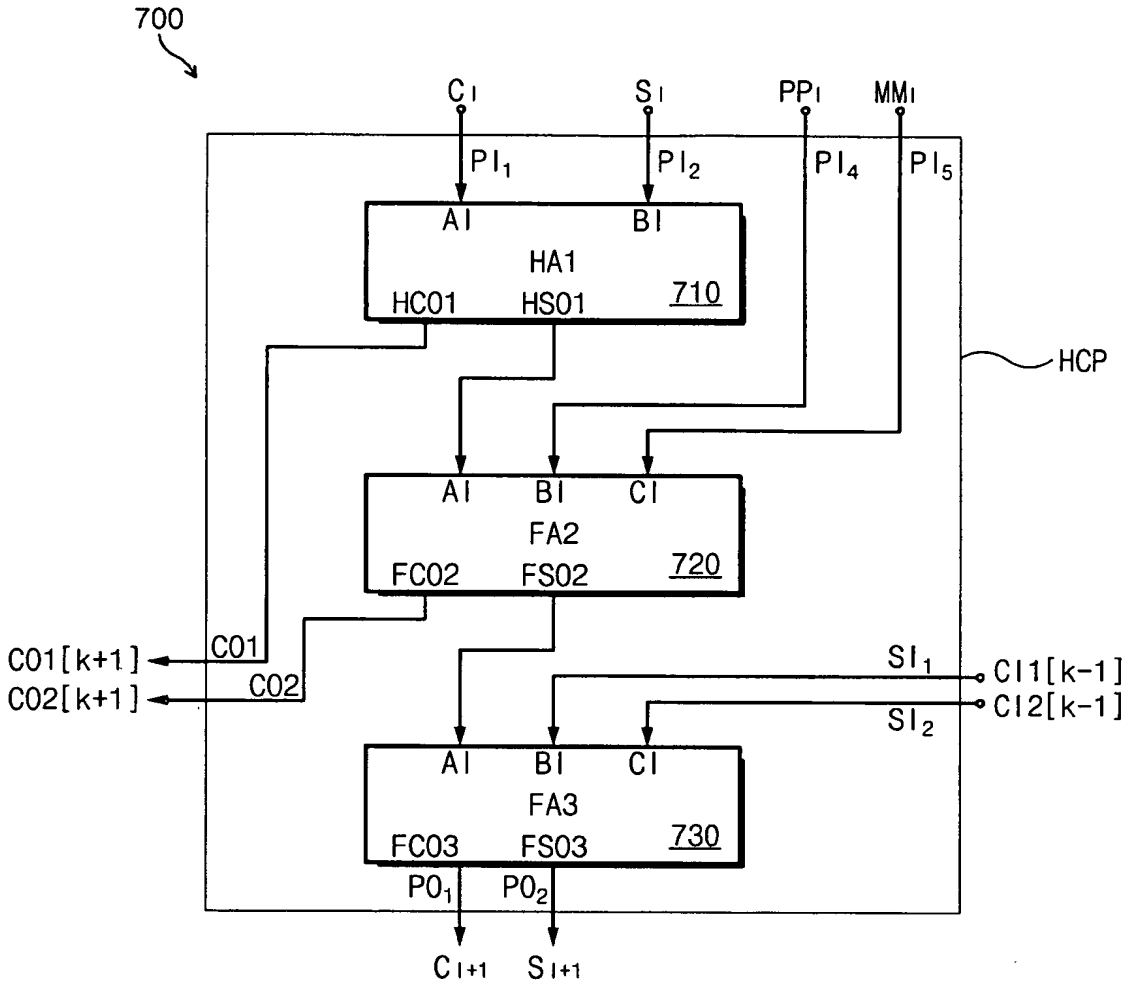

600
CI
SI
CW
PPI
MMI
PI1
PI2
PI3
PI4
PI5
AI
BI
CI
FA1
FC01
FS01
610
FCP
AI
BI
CI
FA2
FC02
FS02
620
C01[k+1]
C01
C02
C02[k+1]
SI1
CI1[k-1]
SI2
CI2[k-1]
AI
BI
CI
FA3
FC03
FS03
630
PO1
PO2
CI+1
SI+1

Fig. 7


700
CI
SI
PPI
MMI
PI1
PI2
PI4
PI5
AI
BI
HA1
HC01
HS01
710
HCP
AI
BI
CI
FA2
FC02
FS02
720
C01[k+1]
C01
C02[k+1]
C02
SI1
CI1[k-1]
SI2
CI2[k-1]
AI
BI
CI
FA3
FC03
FS03
730
PO1
PO2
CI+1
SI+1

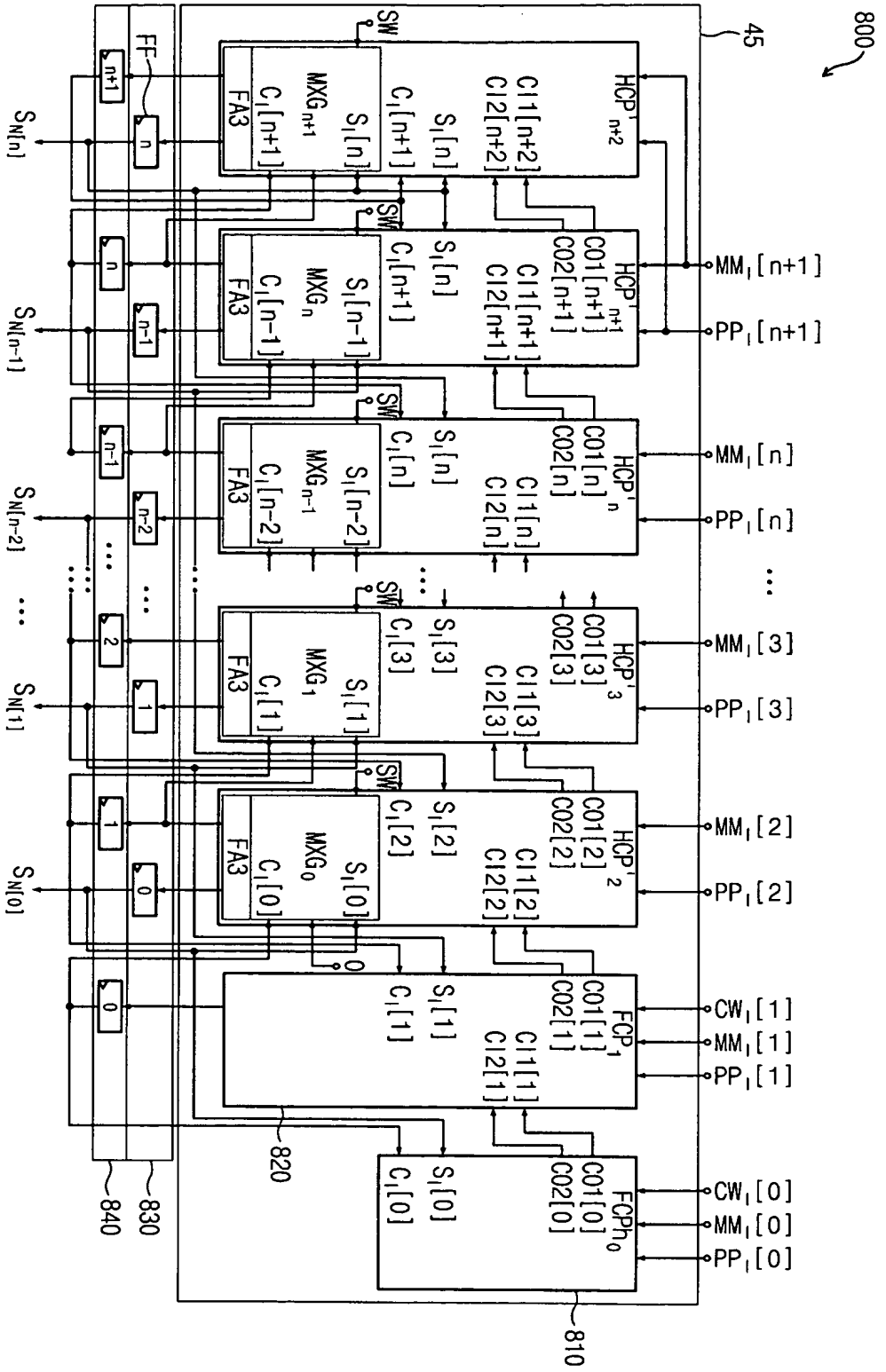

800
45
SW
FF
HCP'n+2
HCP'n+1
HCP'n
HCP'3
HCP'2
FCP1
FCPh0
MXGn+1
MXGn
MXGn-1
MXG1
MXG0
FA3
CI1[n+2]
CI2[n+2]
CI1[n+1]
CI2[n+1]
CI1[n]
CI2[n]
CI1[3]
CI2[3]
CI1[2]
CI2[2]
CI1[1]
CI2[1]
CO1[n+1]
CO2[n+1]
CO1[n]
CO2[n]
CO1[3]
CO2[3]
CO1[2]
CO2[2]
CO1[1]
CO2[1]
CO1[0]
CO2[0]
MM1[n+1]
PP1[n+1]
MM1[n]
PP1[n]
MM1[3]
PP1[3]
MM1[2]
PP1[2]
CW1[1]
MM1[1]
PP1[1]
CW1[0]
MM1[0]
PP1[0]
SN[n]
SN[n-1]
SN[n-2]
SN[1]
SN[0]
820
830
840
810

Fig. 8

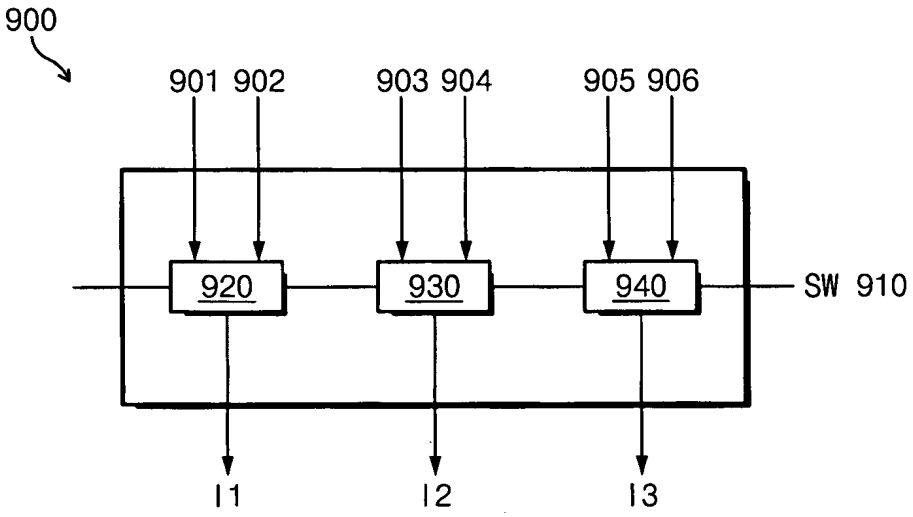



Fig. 9